CLAIMS

1 A data processing apparatus adapted for performing scramble processing of transmit data,

the data processing apparatus comprising:

scramble operation processing means including plural stages of shift registers, and a cyclic operation processing circuit for performing a predetermined operation processing on the basis of a hold value of a predetermined stage of the shift registers and the transmit data to generate scramble-processed data, and to sequentially input the scramble-processed data to the input stage of the shift register;

data generating means for generating bit data of a predetermined pattern; and

switching means supplied with the scramble-processed data and the bit data of the predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data, and to select the scramble-processed data when synchronization processing of transmit data is not performed to output the data thus selected as scrambler output data.

2 The data processing apparatus as set forth in claim 1,

wherein the data generating means is caused to be of the configuration to load the bit data of the predetermined pattern into the shift register at the

time of synchronization processing of transmit data.

3 The data processing apparatus as set forth in claim 1 or 2,

wherein the switching means is caused to be of the configuration in which in the case where a predetermined synchronization pattern data inserted into the transmit data for the purpose of taking synchronization of the transmit data is inserted in the transmit data, the switching means serves to select the bit data of the predetermined pattern to output the bit data thus selected as scrambler output data.

4 The data processing apparatus as set forth in claim 1,

wherein the data generating means is caused to be of the configuration to generate bit data of a predetermined pattern to which predetermined information is assigned in advance.

5 A data processing apparatus adapted for performing scramble processing of transmit data,

the data processing apparatus comprising:

cyclic code generating means for generating cyclic bit data train of a predetermined period;

EXOR operation means for sequentially performing EXOR operation of the cyclic bit data train with respect to the transmit data to output scramble-processed data;

data generating means for generating bit data of a predetermined

pattern; and

switching means supplied with the scramble-processed data and bit data of a predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data, and to select the scramble-processed data when synchronization processing of the transmit data is not performed to output the data thus selected as scrambler output data.

6 The data processing apparatus as set forth in claim 5,

wherein the switching means is caused to be of the configuration in which in the case where a predetermined synchronization pattern data inserted into the transmit data for the purpose of taking synchronization of the transmit data is inserted in the transmit data, the switching means serves to select the bit data of the predetermined pattern to output the bit data thus selected as scrambler output data.

7 The data processing apparatus as set forth in claim 5,

wherein the data generating means is caused to be of the configuration to generate bit data of a predetermined pattern to which predetermined information is assigned in advance.

8 A data reception processing apparatus adapted for performing descramble processing of receive data,

the data reception processing apparatus comprising:

detecting means for detecting bit data of a predetermined pattern for synchronization from the receive data; and

descramble operation processing means including plural stages of shift registers, and a cyclic operation processing circuit for performing a predetermined operation processing on the basis of a hold value of a predetermined stage of the shift registers and the receive data to output descramble-processed data, and to sequentially input the descramble-processed data to the input stage of the shift registers,

wherein the detecting means is caused to be of the configuration in which in the case where the bit data of the predetermined pattern is detected, the detecting means loads the bit data of the predetermined pattern into the shift register.

9 The data reception processing apparatus as set forth in claim 8,

wherein the detecting means is caused to be of the configuration to specify information assigned in advance to the bit data of the predetermined pattern.